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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,033	02/27/2004	Michael Bauer	I431.103.101/FIN 423 US	8344

7590 10/19/2005

Dicke, Billig & Czaja, PLLC
Fifth Street Towers
100 South Fifth Street, Suite 2250
Minneapolis, MN 55402

EXAMINER	
SEFER, AHMED N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/789,033	BAUER ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed July 25, 2005 has been entered and claims 16 and 17 have been cancelled.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, **the conductor track structure** recited in claim 12 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Gebauer et al. ("Gebauer") US PG-Pub 2002/0094607.

Gebauer discloses in figs. 1-10 a semiconductor wafer 20 having a top side and a rear side, the semiconductor wafer comprising: integrated circuits for semiconductor chips 1 arranged in rows 15 and columns 16 on the wafer top side; strip-type separating regions 17 being arranged between the integrated circuits of the semiconductor chips; and wherein the separating regions have passage contacts 18 in the direction of the rear side of the semiconductor wafer.

Regarding claims 2 and 3, Gebauer discloses passage contacts having perforations, wherein the perforations have walls 11 having a metal layer 12/25 applied thereto (as in claim 3).

5. Claim 6-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamaguchi US PG-Pub 2004/0157410.

Yamaguchi discloses in figs. 1-13 a semiconductor chip with a top side, a rear side, and with edge sides, the semiconductor chip comprising: an integrated circuit (par. 0182) on the top side; at least one edge side having edge contacts 11/98 wherein, the edge contacts extend from

the top side in the direction of the rear side of the semiconductor chip; and wherein the edge contacts are connected to electrodes 2/92 of the integrated circuit via conductor tracks 3/93 located on the top surface of the semiconductor chip.

Regarding claims 7 and 8, Yamaguchi discloses edge sides having a perforation-like structure, semicylinder-like cutouts extending as edge contacts from the top side in the direction of the rear side, and having a metal layer 6/96 or an insulating layer 5/95 (as in claim 8).

Regarding claim 9, Yamaguchi discloses (par. 0169) cutouts having a soldering material.

Regarding claim 10, Yamaguchi discloses edge contacts being extended on the top side to form a contact area and merge with a conductor track on the top side.

Regarding claim 11, Yamaguchi discloses (par. 0061 and claim 10) a semiconductor chip arranged on a circuit substrate within an electronic component.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gebauer in view of Yamaguchi.

Gebauer discloses the device structure as recited in the claim, but does not specifically disclose walls having an insulation layer.

Yamaguchi discloses in figs. 1-13 a semiconductor chip with a top side, a rear side, and with edge sides, the semiconductor chip comprising: an integrated circuit (par. 0182); and

passage contacts having perforations having walls wherein the walls have an insulation layer 5.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify Gebauer's device by incorporating walls have an insulation layer since that would provide a high connection reliability as taught by Yamaguchi.

Regarding claim 5, Yamaguchi discloses (par. 0169) passage contacts having fusible solder material.

8. Claim 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi in view of Glenn et al. ("Glenn") USPN 6,406,934.

Yamaguchi discloses the device structure as recited in the claim, but does not specifically disclose a circuit substrate having a conductor track structure.

Glenn discloses (figs. 3-6 and col. 42-49) a semiconductor chip with a top side, a rear side, and with edge sides, the semiconductor chip comprising a circuit substrate having a conductor track structure, the semiconductor chip being arranged with its rear side on the top side or in angular fashion (as in claim 14) of the circuit substrate and edge contacts being electrically connected to the conductor track structure via contact pads 46 on the top side of the circuit substrate.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify Yamaguchi's device by incorporating a conductor track structure since that would reduce cost, size and complexity in manufacturing process as taught by Glenn.

Regarding claim 13, Glenn discloses insulating plastics composition 48 being arranged on the substrate in a manner embedding the edge sides of the chip and contact paths.

Regarding claim 15, Yamaguchi discloses plurality of chips being stacked one on the other and being electrically connected via the edge contact among one another and also with respect to external contacts.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
October 12, 2005

NATHAN J. FLYNN
SUPERVISORY PATENT
TECHNOLOGY